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Using Verilog RTL Models; To Do On Your Own; Introduction. This tutorial will discuss the various views that make-up a standard-cell library and then illustrate how to use a set of Synopsys and Cadence ASIC tools to map an RTL design down to these standard cells and ultimately silicon. The tutorial will discuss the key tools used for synthesis ...

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Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL. While these languages are capable of defining ...

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606.2 KB: ABEL-HDL Reference Manual ...

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Intro - Verilator - Veripool

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